IDEC Chip Design Contest

Measurement and Analysis of Power Distribution Network (PDN) Noise Coupling Paths on Chip

Shinyoung Park[1], Subin Kim[1], and and Joungho Kim[2]
School of Electrical Engineering, Korea Advanced Institute of Science and Technology
E-mail : shinyoung.park@kaist.ac.kr

Introduction

- The increase in the data bandwidth requires a large number of I/O buffers switch at a faster rate with higher drive strength, which ultimately raise simultaneously switching output (SSO) noise problem in the systems.
- Designing PDNs with in-depth understanding of the PDN noise coupling according to the on-chip PDN designs is important.
- In this paper, we designed four different on-chip PDNs, measured and analyzed their PDN noise coupling paths in terms of self impedance and transfer impedance.

Design of On-Chip PDNs

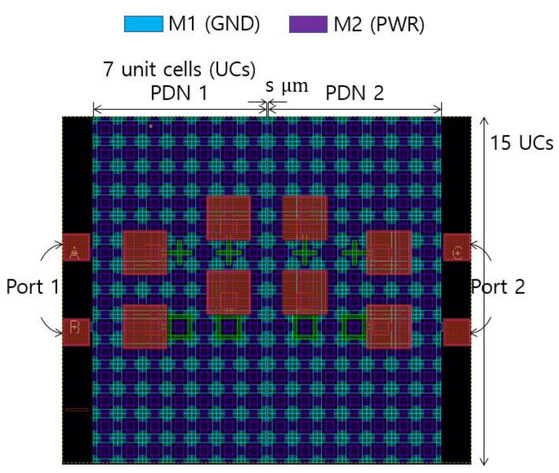
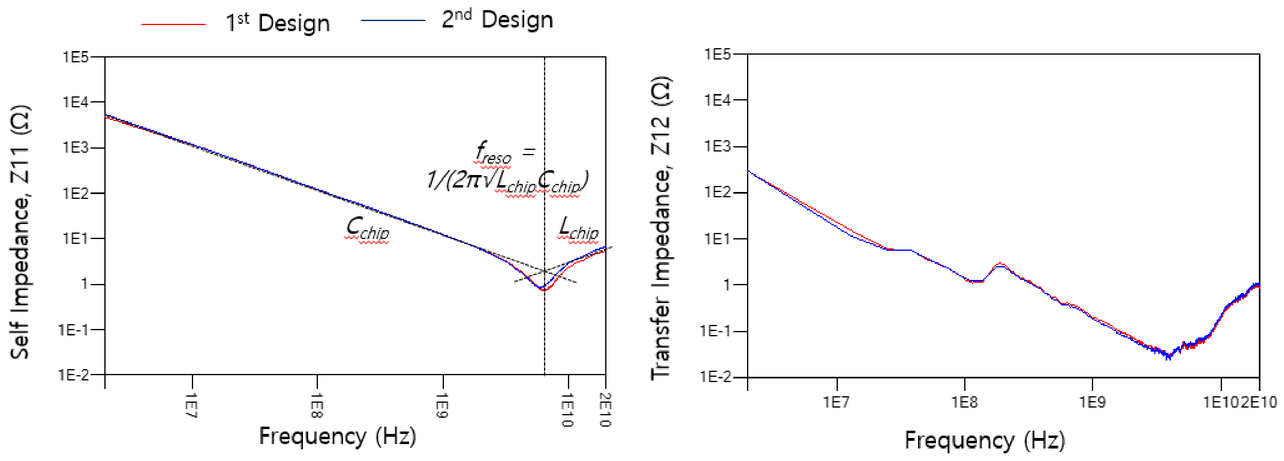


Fig. 1 Four different on-chip PDN designs.
(a) The ground rails are shared, but the power rails are separated (s = 5 μm), (s = 10 μm). (c) Both of the power and ground rails are separated (s = 5 μm)

- We designed four different on-chip PDNs.
- Power and ground rails were placed on M1 and M2 layers, respectively.
- The PDNs were designed into heavily perforated structure because it is typical of cost reduced and low-layer count structure.

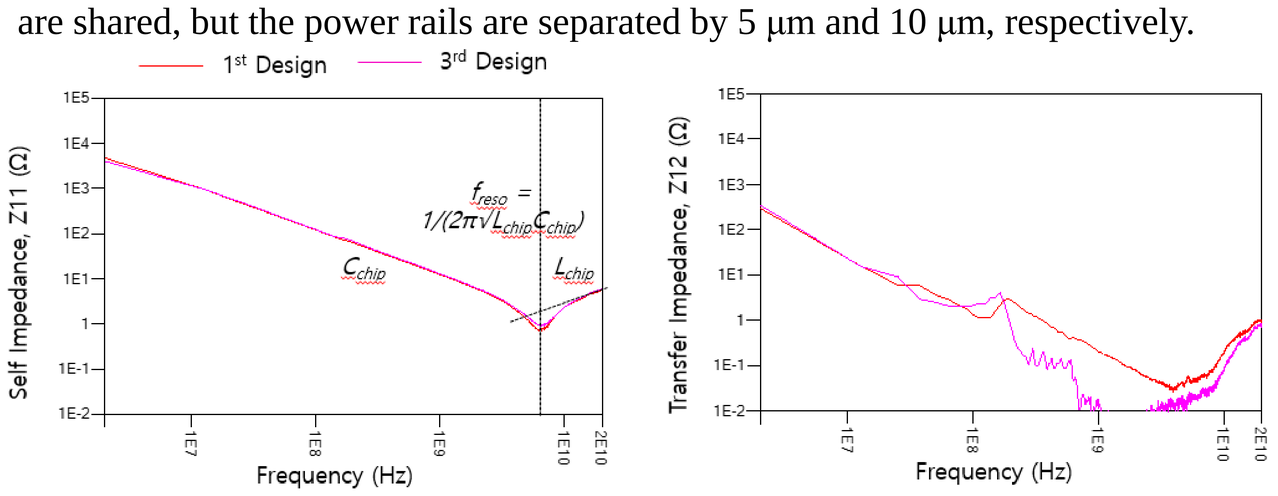
Analysis of the Noise Coupling Paths on the Designed On-Chip PDNs



(a) (b)

Fig. 2. Comparison of (a) Z11 and (b) Z12 of the on-chip PDNs which ground rails are shared, but the power rails are separated by 5 μm and 10 μm, respectively.

- The impact of distance of PDNs was analyzed.
- Fig.2 showed that the self-generated noise of PDN 2 propagated to PDN 1 through the parasitic capacitance and through the shared ground rails.
- Since the parasitic capacitance formed by the overlapping regions of the separated power rails of PDN 1 and PDN 2 and the inductance of the shared ground rails were similar, their Z12 profiles were almost the same.
- The results show that the distance between the power rails has little impact on the noise coupling between the PDNs.



(a) (b)

Fig. 3. Comparison of (a) Z11 and (b) Z12 of the on-chip PDN which ground rails a re shared, but the power rails are separated by 5 μm and the on-chip PDN which bo th power and ground rails are separated by 5 μm.

- The impact of ground rail separation was analyzed.
- Since the size of the PDNs of the 1st design and the 2nd design were similar, their Z11 profiles were almost the same.
- On the other hand, the 2nd design showed lower Z12 compared to the 1st design.
- As the ground rails were separated, the noise coupling through the ground were removed.
- Since the separation of the ground has no impact on Z11 while it reduces Z12, it is better to separate ground network between the PDNs.

Conclusion

- Compared to the design that had separated power rails and unified ground rails, the design that had both separated power and ground rails showed similar self impedance and smaller transfer impedance.
- To prevent the SSO noise coupling to the other power domains, on-chip power/ground rails of an I/O PDN and the others are usually separated. However, it will increase the overall impedance of the PDNs.
- Therefore, it is important to design the PDNs in considerations of in-depth understanding of the PDN noise coupling according to the on-chip PDN designs.